HP's IOP Implementations: 2100 vs 21MX

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Summary

HP's Access system (a late version of TimeShared Basic) consisted of two processors linked by a parallel interconnect. One of the computers was responsible for computation and mass storage and was called the System Processor; the other was responsible for character-by-character I/O and was called the I/O processor. To improve performance, the IOP used unique microcode assists called the IOP instruction set. On the HP 2100, these instructions overlapped with, and were mutually exclusive with, the floating point microcode. On the HP 21MX, these instructions occupied different code points in the extended instruction space.

Encoding Differences

Instruction	2100	21MX	notes
ILIST	105000	105470	
LAI	105020-57	105400-37	
SAI	105060-117	101400-37	
MBYTE	105120	105765	standard 21MX instruction
CRC	105150	105460	
TRSLT	105160	105467	not used in 21MX IOP code
MWORD	105200	105777	standard 21MX instruction
READF	105220	105462	
PRFIO	105221	105473	
PRFEI	105222	105471	
PRFEX	105223	105472	
ENQ	105240	105464	
PENQ	105257	105465	
DEQ	105260	105466	
SBYTE	105300	105764	standard 21MX instruction
LBYTE	105320	105763	standard 21MX instruction
REST	105340	105461	
SAVE	105362	105474	
INS	-	105463	

Functional Differences

1. The 2100's byte and word move instructions have the same functional definition as the 21MX's standard MVB and MVW, but the 2100's microcode implementation checked an additional condition (do nothing if the count is less than zero).

2. The 2100 uses the memory protect option's fence register (internally, the F register) as the IOP stack pointer. The F register is loaded with an OTx 5 instruction, and stored with READF. The 21MX uses a different internal register, because it provides a new instruction to load the stack pointer.
3. The 2100's TRSLT instruction is not used in the 21MX IOP code, even though the code point is defined.